Claim 1 (**Currently Amended**) A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed over said semiconductor substrate,

a capacitor formed over said first insulating film, and having a capacitor dielectric film and a pair of electrodes sandwiching the capacitor dielectric film, one of the electrodes having ~~one electrode which includes~~ an extension ~~extending~~ selectively extending beyond an edge of the other electrode and extending over said first insulating film;

a second insulating film formed over said first insulating film;

a first contact hole penetrating through said second insulating film and said extension of the one electrode, but not touching the other electrode; and

a first conductor pattern burying said first contact hole.

Claim 2 (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed over said semiconductor substrate;

a first conducting plug formed in said first insulating film;

a storage electrode formed over said first insulating film, and electrically connected to said conducting plug;

a capacitor dielectric film formed over said storage electrode;

an opposing electrode formed over said capacitor dielectric film, and having an extension selectively extending beyond an edge of the storage electrode and extending over said first insulating film;

a second insulating film formed over said opposing electrode;

a first contact hole penetrating through said second insulating film and said extension of the opposing electrode, but not touching the storage electrode; and

a first conductor pattern burying said contact hole.

Claim 3 (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a switching transistor including an insulated gate formed on the substrate and source/drain regions formed in the substrate on both sides of the insulated gate;

an insulator laminate formed on the substrate, and including a lower part covering said insulated gate and a higher part formed over the lower part;

a first conductive plug formed through the lower part of the insulator laminate and connected to one of the source/drain regions;

a storage electrode formed in the higher part of the insulating laminate and electrically connected to the first ~~conducting~~ conductive plug;

a capacitor dielectric layer formed on the storage electrode;

an opposing electrode covering the capacitor dielectric layer and having an extension selectively extending beyond an edge of the storage electrode and formed over the lower part of the insulator laminate;

a lower conducting member formed within the lower part of the insulator laminate;

a second conductive plug penetrating through the higher part of the insulating laminate and the extension of the opposing electrode and electrically connected to the opposing electrode at a side surface, but not touching the storage electrode;

a third conductive plug formed through the insulator laminate above said lower conductive member, and electrically connected to an upper surface of the lower conductive member.

Claim 4 (Original) The semiconductor memory device according to claim 3, wherein said lower part of the insulator laminate includes a silicon nitride layer at an uppermost level.

Claim 5 (Previously Presented) The semiconductor memory device according to claim 4, wherein said silicon nitride layer is patterned to have a same planar shape as the opposing electrode.

Claim 6 (Original) The semiconductor memory device according to claim 3, wherein said storage electrode has a cylinder shape.

Claim 7 (Original) The semiconductor memory device according to claim 6, wherein said storage electrode is formed of a silicon layer.

Claim 8 (Original) The semiconductor memory device according to claim 3, wherein said higher part of the insulator laminate has a planarized upper surface.

Claim 9 (Original) The semiconductor memory device according to claim 8, wherein said second and third plugs are contiguous to wiring pattern formed over the higher part of the insulator laminate.

Claim 10 (Original) The semiconductor memory device according to claim 3, wherein said opposing electrode is formed of a silicon layer.

Claim 11 (Previously Presented) The semiconductor memory device according to claim 10, wherein said lower part of the insulator laminate includes a silicon nitride layer at an uppermost level, which is patterned after the opposing electrode.

Claim 12 (Original) The semiconductor memory device according to claim 10, wherein said lower conducting member includes a metal silicide layer at its top level.

Claim 13 (Original) The semiconductor memory device according to claim 3, further comprising a fourth conducting plug formed through the insulator laminate and reaching the semiconductor substrate.

Claim 14 (Original) The semiconductor memory device according to claim 12, wherein said lower conducting member has oxide side walls and a silicon nitride layer covering the metal suicide layer and the oxide side walls.

Claim 15 (Original) The semiconductor memory device according to claim 3, wherein

said insulated gate comprises a gate insulating layer formed on the semiconductor substrate, a gate silicon layer formed on the gate insulating layer, a gate suicide layer formed on the gate silicon layer, oxide side walls formed on side surfaces of the gate silicon layer and the gate suicide layer, and a gate silicon nitride layer covering the gate silicon layer and the oxide side walls.

Claim 16 (Original) The semiconductor memory device according to claim 15, wherein said first conducting plug is contiguous to the gate silicon nitride layer.

Claim 17 (Original) The semiconductor memory device according to claim 3, further comprising:

a fifth conducting plug formed through the lower part of said insulator laminate and connected to another of said source/drain regions; and

a bit line formed over the lower part of and in the higher part of said insulator laminate and connected to said fifth conducting plug.

Claim 18 (Previously Presented) The semiconductor memory device according to claim 17, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the oxide side walls of the bit line.

Claim 19 (Original) The semiconductor memory device according to claim 18, wherein said storage electrode is contiguous to said bit silicon nitride layer.

Claim 20 (Original) The semiconductor memory device according to claim 18, wherein said conducting bit layer includes a silicon bit layer and a silicide bit layer formed on the silicon bit layer.

Claim 21 (Original) The semiconductor memory device according to claim 18, further comprising:

a medium conducting member formed over the lower part of and in the higher part of said insulator laminate.

Claim 22 (Original) The semiconductor memory device according to claim 21, wherein said medium conducting member comprises a common structure as said bit line.

Claim 23 (Original) The semiconductor memory device according to claim 22, further comprising a sixth conducting plug formed through the higher part of said insulator laminate and the silicon nitride layer of the medium conducting member, and connected to the silicide layer of the medium conducting member.

Claim 24 (Previously Presented) The semiconductor device according to claim 1, further comprising:

a wiring layer formed on the semiconductor substrate and covered with said first insulating film;

a second contact hole formed through said first and second insulating films to reach a surface of said wiring layer; and

a second conductor pattern burying said second contact hole.

Claim 25 (Previously Presented) The semiconductor device according to claim 24, further comprising:

an impurity diffusion region formed in said semiconductor substrate and connected to said wiring layer;

a third contact hole formed through said second and first insulating film, and reaching said impurity diffusion region; and

a third conductive pattern burying said third contact hole.

Claim 26 (Previously Presented) The semiconductor device according to claim *25,* further comprising:

a switching transistor including an insulated gate formed on the substrate, and covered with said first insulating film, and source/drain regions formed in the substrate on both sides of the insulated gate; and

a first conductive plug formed through the first insulating film and connected to said one electrode of the capacitor and one of said source/drain regions.

Claim 27 (Previously Presented) The semiconductor device according to claim 26, wherein said insulated gate comprises a gate insulating layer formed on the semiconductor substrate, a gate silicon layer formed on the gate insulating layer, a gate silicide layer formed on the gate silicon layer, oxide side walls formed on side surfaces of the gate silicon layer and the gate silicide layer, and a gate silicon nitride layer covering the gate silicon layer and the oxide side walls.

Claim 28 (Previously Presented) The semiconductor memory device according to claim 27, wherein said first conducting plug is contiguous to the gate silicon nitride layer.

Claim 29 (Previously Presented) The semiconductor memory device according to claim 28, further comprising:

a second conducting plug formed through said first insulating film and connected to another of said source/drain regions; and

a bit line formed over the first insulating film and in the second insulating film and connected to said second conducting plug.

Claim 30 (Previously Presented) The semiconductor memory device according to claim 29, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the oxide side walls of the bit line.

Claim 31 (Previously Presented) The semiconductor device according to claim 2, further comprising:

a wiring layer formed on the semiconductor substrate and covered with said first insulating film;

a second contact hole formed through said first and second insulating films to reach a surface of said wiring layer; and

a second conductor pattern burying said second contact hole.

Claim 32 (Previously Presented) The semiconductor device according to claim 31, further comprising:

an impurity diffusion region formed in said semiconductor substrate and connected to said wiring layer;

a third contact hole formed through said second and first insulating film, and reaching said impurity diffusion region; and

a third conductive pattern burying said third contact hole.

Claim 33 (Previously Presented) The semiconductor device according to claim 32, further comprising:

a switching transistor including an insulated gate formed on the substrate, and covered with said first insulating film, and source/drain regions formed in the substrate on both sides of the insulated gate;

wherein said first conducting plug is formed through the first insulating film and electrically connected to one of said source/drain regions.

Claim 34 (Previously Presented) The semiconductor device according to claim 33, wherein said insulated gate comprises a gate insulating layer formed on the semiconductor substrate, a gate silicon layer formed on the gate insulating layer, a gate silicide layer formed on the gate silicon layer, oxide side walls formed on side surfaces of the gate silicon layer and the gate suicide layer, and a gate silicon nitride layer covering the gate silicon layer and the oxide side walls.

Claim 35 (Previously Presented) The semiconductor memory device according to claim 34, wherein said first conducting plug is contiguous to the gate silicon nitride layer.

Claim 36 (Previously Presented) The semiconductor memory device according to claim 35, further comprising:

a second conducting plug formed through said first insulating film and connected to another of said source/drain regions; and

a bit line formed over the first insulating film and in the second insulating film and connected to said second conducting plug.

Claim 37 (Previously Presented) The semiconductor memory device according to claim 36, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the oxide side walls of the bit line.

Claim 38 (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell transistor having impurity doped regions and a gate electrode;

an insulator laminate formed over said semiconductor substrate, and including a lower part covering said memory cell transistor and an upper part formed over said lower part;

a first contact hole, formed through said lower part of said insulator laminate, exposing one of said impurity doped regions;

a first conductor filled in said first contact hole and electrically connected to one of said impurity doped regions;

a storage electrode formed in said upper part of said insulating laminate and electrically connected to said first conductor;

a capacitor insulating film formed on said storage electrode;

an opposing electrode covering said capacitor insulating film and having an extension selectively extending beyond an edge of the storage electrode and formed over said lower part of said insulator laminate;

a second contact hole, formed through said upper part of said insulating laminate, penetrating through said extension of said opposing electrode, but not touching the storage electrode;

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at its side wall exposed in said second contact hole;

a third contact hole, formed in said insulating laminate, exposing a third conductor and being deeper than said second contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to a surface of said third conductor.

Claim 39 (Previously Presented) A semiconductor memory device according to claim 38, wherein said third conductor is disposed in said lower part of said insulating laminate.

Claim 40 (Previously Presented) A semiconductor memory device according to claim 38,

wherein said third conductor is an impurity doped region formed in said semiconductor substrate.

Claim 41 (Previously Presented) A semiconductor memory device according to claim 38, wherein said lower part of said insulator laminate includes a nitride film at an uppermost level.

Claim 42 (Previously Presented) A semiconductor memory device according to claim 38, wherein said storage electrode is a cylinder type storage electrode.

Claim 43 (Previously Presented) A semiconductor memory device according to claim 38, wherein said opposing electrode is composed of a polysilicon and said third conductor is a metal silicide.

Claim 44 (Previously Presented) A semiconductor memory device according to claim 38, wherein said upper part of said insulator laminate has a planarized upper surface.

Claim 45 (Previously Presented) A semiconductor memory device according to claim 39, wherein a first nitride film is disposed between said opposing electrode and said semiconductor substrate, and said third conductor is covered with a second nitride film.

Claim 46 (Previously Presented) A semiconductor memory device according to claim 38 further comprising:

a fourth contact hole, formed through said insulator laminate, exposing said semiconductor substrate and being deeper than said third contact hole; and

a fifth conductor filled in said fourth contact hole and electrically connected to said semiconductor substrate,

wherein said third conductor is disposed in said lower part of said insulator laminate.

Claim 47 (Currently Amended) A semiconductor memory device comprising:

a first insulator formed over a semiconductor substrate;

a memory cell transistor;

a memory cell capacitor, formed over said first insulator, having a first electrode electrically connected to said memory cell transistor, a capacitor insulating film and a second electrode, the second electrode selectively extending beyond an edge of the first electrode and extending over said first insulator;

a second insulator covering said memory cell transistor and said memory cell capacitor;

a contact hole penetrating through said second insulator and said second electrode to form a side wall of the second electrode exposed at a side wall of the contact hole, but not touching the first electrode; and

a conductor, filled in said contact hole, for applying a predetermined potential to said second electrode, wherein said conductor is electrically connected to said second electrode at the side wall formed by penetration of said contact hole.

Claim 48 (Previously Presented) A semiconductor memory device according to claim 47, wherein said first electrode is a cylinder type storage electrode having a bottom portion electrically connected to said memory cell transistor and a cylindrical portion extending upwardly.

Claim 49 (Previously Presented) A semiconductor memory device according to claim 48, wherein a height of said cylinder type storage electrode is larger than its width.

Claim 50 (Currently Amended) A semiconductor memory device comprising:

a first insulator formed over a semiconductor substrate;

a wiring disposed in said first insulator;

a memory cell transistor;

a memory cell capacitor, formed over said first insulator, having a first electrode electrically connected to said memory cell transistor, a capacitor insulating film and a second electrode, the second electrode selectively extending beyond an edge of the first electrode and extending over said first insulator;

a second insulator covering said memory cell transistor and said memory cell capacitor;

a first contact hole penetrating through said second insulator and said second electrode to form a side wall of the second electrode exposed at a side wall of the contact hole, but not touching the first electrode;

a first conductor, filled in said first contact hole, for applying a predetermined potential to said second electrode, wherein said first conductor is electrically connected to said second electrode at its side wall formed by penetration of said contact hole;

a second contact hole exposing a surface of said wiring through said first and second insulators; and

a second conductor filled in said second contact hole, wherein said second conductor is electrically connected to said wiring at said surface.

Claim 51 (Previously Presented) A semiconductor memory device according to claim 50, wherein said second electrode is composed of a different conductive material from a conductive material of said wiring.

Claim 52 (Previously Presented) A semiconductor memory device according to claim 50, wherein said second electrode is composed of a polysilicon, and said wiring is a metal silicide.

Claim 53 (Previously Presented) A semiconductor memory device according to claim 50, further comprising a third insulator, disposed between said second electrode and said semiconductor substrate, having etching characteristics different from that of said second insulator.

Claim 54 (Previously Presented) A semiconductor memory device according to claim 53, wherein said third insulator is composed of a nitride film.

Claim 55 (Previously Presented) A semiconductor memory device according to claim 50, wherein said wiring is covered with a nitride film.

Claim 56 (Previously Presented) A semiconductor memory device according to claim 50, wherein said first contact hole is located in a memory cell area, said second contact hole is located in a peripheral circuit area.

Claim 57 (Previously Presented) A semiconductor memory device according to claim 50, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.

Claim 58 (Currently Amended) A semiconductor memory device comprising:

a first insulator formed over a semiconductor substrate;

a wiring disposed in said first insulator;

an impurity doped region formed in said semiconductor substrate;

a memory cell transistor;

a memory cell capacitor, formed over said first insulator, having a first electrode electrically connected to said memory cell transistor, a capacitor insulating film and a second electrode, the second electrode selectively extending beyond an edge of the first electrode and extending over said first insulator;

a second insulator covering said memory cell transistor and said memory cell capacitor;

a first contact hole penetrating through said second insulator and said second electrode to form a side wall of the second electrode exposed at a side wall of the contact hole, but not touching the first electrode;

a first conductor, filled in said first contact hole, for applying a predetermined potential to said second electrode, wherein said first conductor is electrically connected to said second electrode at the side wall formed by penetration of said first contact hole;

a second contact hole exposing a surface of said wiring through said first and second insulators;

a second conductor filled in said second contact hole, wherein said second conductor is electrically connected to said wiring at said surface;

a third contact hole exposing a surface of said impurity doped region through said first and second insulators; and

a third conductor filled in said third contact hole, wherein said third conductor is electrically connected to said impurity doped region at said surface.

Claim 59 (Previously Presented) A semiconductor memory device according to claim 58, wherein said second electrode is composed of a different conductive material from a conductive material of said wiring.

Claim 60 (Previously Presented) A semiconductor memory device according to claim 58, wherein said second electrode is composed of a polysilicon, and said wiring is a metal silicide.

Claim 61 (Previously Presented) A semiconductor memory device according to claim 58, further comprising a third insulator, disposed between said second electrode and said semiconductor substrate, having etching characteristics different from that of said second insulator.

Claim 62 (Previously Presented) A semiconductor memory device according to claim 61, wherein said third insulator is composed of a nitride film.

Claim 63 (Previously Presented) A semiconductor memory device according to claim 58, wherein said wiring is covered with a nitride film.

Claim 64 (Previously Presented) A semiconductor memory device according to claim 58, wherein said first contact hole is located in a memory cell area, and said second and third contact holes are located in a peripheral circuit area.

Claim 65 (Previously Presented) A semiconductor memory device according to claim 58, wherein said first contact hole is located in a memory cell area, and said second and third contact holes are located in a peripheral circuit area.

Claim 66 (Previously Presented) A semiconductor memory device according to claim 58, wherein a third insulator is disposed between said second electrode and said semiconductor substrate, said wiring is covered with a fourth insulator, and said third and fourth insulators have different etching characteristics from that of said second insulator.

Claim 67 (Previously Presented) A semiconductor memory device according to claim 66, wherein said third insulator is composed of a first nitride film, and said fourth insulator is composed of a second nitride film.

Claim 68 (Previously Presented) A semiconductor memory device according to claim *58*, wherein said first electrode is a cylinder type storage electrode having a bottom portion

electrically connected to said memory cell transistor and a cylindrical portion extending upwardly.

Claim 69 (Previously Presented) A semiconductor memory device according to claim 68, further comprising a third insulator, disposed between said second and first insulators, having an opening, wherein said bottom portion of said cylinder type storage electrode is disposed in said opening and said cylindrical portion is disposed in said second insulator.

Claim 70 (Previously Presented) A semiconductor memory device according to claim 68, wherein said cylinder type storage electrode has a height larger than its width.

Claim 71 (Previously Presented) A semiconductor memory device according to claim 69, wherein said second electrode is extending over said third insulator.

Claim 72 (Previously Presented) A semiconductor memory device according to claim 58, wherein each of said first and second insulators has a planarized surface.

Claim 73 (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell transistor having a gate electrode and impurity doped regions formed in said semiconductor substrate;

a first insulator formed over said semiconductor substrate covering said memory cell transistor and having a planarized surface;

a first contact hole, formed through said first insulator, exposing one of said impurity doped regions;

a first conductor filled in said first contact hole;

a second insulator, formed over said first insulator, having a planarized surface and an opening exposing said first conductor;

a memory cell capacitor having a cylinder type storage electrode electrically connected to said one of said impurity doped regions via said first conductor, a capacitor insulation film and an opposing electrode,

wherein said cylinder type storage electrode has a lower portion disposed in said opening and an upper portion extending upwardly, said opposing electrode faces said cylinder type storage electrode via said capacitor insulating film and selectively extends beyond an edge of the cylinder type storage electrode and extends over said second insulator;

a third insulator formed over said second insulator, covering said memory cell capacitor and having a planarized surface;

a second contact hole penetrating through said third insulator and said opposing electrode disposed over said second insulator to form a side wall of the opposing electrode exposed at a side wall of the second contact hole, but not touching the cylinder type storage electrode,

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at the side wall formed by penetration of said second contact hole;

a third contact hole of which a depth from said planarized surface of said third insulator is larger than a depth of said second contact hole; and

a third conductor having a surface exposed in said third contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to said third conductor at its surface.

Claim 74 (Previously Presented) A semiconductor memory device according to claim 73, wherein said third conductor is disposed in said first insulator.

Claim 75 (Previously Presented) A semiconductor memory device according to claim 73, wherein said third conductor is an impurity doped region formed in said semiconductor substrate.

Claim 76 (Previously Presented) A semiconductor memory device according to claim 73, further comprising a field insulating film between said semiconductor substrate and said first insulator, wherein said third conductor is formed over said field insulating film.

Claim 77 (Previously Presented) A semiconductor memory device according to claim 73, wherein a diameter of said opening of said second insulator is larger than a diameter of said first contact hole.

Claim 78 (Previously Presented) A semiconductor memory device according to claim 73, wherein a height of said cylinder type storage electrode is larger than its width.

Claim 79 (Previously Presented) A semiconductor memory device according to claim 73, wherein said cylinder type storage electrode has an inner wall and an outer wall facing said opposing electrode via a capacitor insulating film.

Claim 80 (Previously Presented) A semiconductor memory device according to claim 73, wherein a fourth insulator is disposed between said second insulator and said opposing electrode, said third conductor is covered with a fifth insulator, and each of said fourth and fifth insulators has different etching characteristics from that of said third insulator.

Claim 81 (Previously Presented) A semiconductor memory device according to claim 73, further comprising wirings, formed over said third insulator and electrically connected to said second and fourth conductors respectively.

Claim 82 (Previously Presented) A semiconductor memory device according to claim 73, further comprising:

a fourth contact hole, formed through said third, second and first insulators, exposing a surface of said semiconductor substrate, and

a fifth conductor filled in said fourth contact hole,

wherein said third conductor is disposed in said first insulator, and a depth of said fourth contact hole is larger than said depth of said third contact hole.

Claim 83 (Previously Presented) A semiconductor memory device according to claim 73, wherein another of said impurity doped regions of said memory cell transistor is electrically connected to a bit line which is composed of a lower conductive layer than said cylinder type storage electrode.

Claim 84 (Previously Presented) A semiconductor memory device according to claim 73,

wherein said opposing electrode is composed of a different conductive material from a conductive material of said third conductor.

Claim 85 (Previously Presented) A semiconductor memory device according to claim 73, wherein said opposing electrode is composed of a polysilicon, and said third conductor is a metal suicide.

Claim 86 (Previously Presented) A semiconductor memory device according to claim 73, further comprising a fourth insulator, disposed between said opposing electrode and said second insulator, having etching characteristics different from that of said third insulator.

Claim 87 (Previously Presented) A semiconductor memory device according to claim 86, wherein said fourth insulator is composed of a nitride film.

Claim 88 (Previously Presented) A semiconductor memory device according to claim 73, wherein said third conductor is covered with a nitride film.

Claim 89 (Previously Presented) A semiconductor memory device according to claim 73, wherein said first and second contact holes are located in a memory cell area, and said third contact hole is located in a peripheral circuit area.

Claim 90 (Previously Presented) A semiconductor memory device according to claim 73, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.

Claim 91 (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of memory cells each comprising a memory cell transistor having a gate electrode and impurity doped regions formed in said semiconductor substrate and a memory cell capacitor having a cylinder type storage electrode electrically connected to said one of said impurity doped regions, a capacitor insulating film and an opposing electrode;

a first insulator, formed over said semiconductor substrate, covering said memory cell transistor and having a planarized surface;

first contact holes, formed through said first insulator, each exposing one of said impurity doped regions of each of said memory cell transistors;

first conductors filled in said first contact holes;

a second insulator, formed over said first insulator, having a planarized surface and openings exposing said each of said first conductors, wherein each said cylinder type

storage electrode has a lower portion disposed in said openings and an upper portion extending upwardly, each said opposing electrode is composed of a common conductive layer facing each said cylinder type storage electrode via said capacitor insulating film and selectively extending beyond an edge of the cylinder type storage electrode and extending over said second insulator;

a third insulator, formed over said second insulator, covering each said memory cell capacitor and having a planarized surface;

a second contact hole penetrating through said third insulator and said common conductive layer disposed over said second insulator to form a side wall of the opposing electrode exposed at a side wall of the second contact hole, but not touching the cylinder type storage electrode;

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at the side wall formed by penetration of said second contact hole;

a third contact hole of which a depth from said planarized surface of said third insulator is larger than a depth of said second contact hole; and

a third conductor having a surface exposed in said third contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to said third conductor at its surface.

Claim 92 (Currently Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell transistor having a gate electrode and impurity doped regions formed in said semiconductor substrate;

a first insulator, formed over said semiconductor substrate, covering said memory cell transistor and having a planarized surface;

a first contact hole, formed through said first insulator, exposing one of said impurity doped regions;

a first conductor filled in said first contact hole;

a memory cell capacitor having a cylinder type storage electrode electrically connected to said one of said impurity doped regions via said first conductor, a capacitor insulating film and an opposing electrode,

wherein said cylinder type storage electrode has a lower portion disposed over said first contact hole and an upper portion extending upwardly, said opposing electrode faces said cylinder type storage electrode via said capacitor insulating film and selectively extends beyond an edge of the cylinder type storage electrode and extends over said first insulator;

a second insulator, formed over said first insulator, covering said memory cell capacitor and having a planarized surface;

a second contact hole penetrating through said second insulator and said opposing electrode disposed over said first insulator to form a side wall of the opposing electrode exposed at a side wall of the second contact hole, but not touching the cylinder type storage electrode;

a second conductor filled in said second contact hole and electrically connected to said opposing electrode at the side wall formed by penetration of said second contact hole;

a third contact hole of which a depth from said planarized surface of said second insulator is larger than a depth of said second contact hole; and

a third conductor having a surface exposed in said third contact hole; and

a fourth conductor filled in said third contact hole and electrically connected to said third conductor at its surface.

Claim 93 (Previously Presented) A semiconductor memory device according to claim 92, wherein said third conductor is disposed in said first insulator.

Claim 94 (Previously Presented) A semiconductor memory device according to claim 92,

wherein said third conductor is an impurity doped region formed in said semiconductor substrate.

Claim 95 (Previously Presented) A semiconductor memory device according to claim 92, further comprising a field insulating film between said semiconductor substrate and said first insulator, wherein said third conductor is formed over said field insulating film.

Claim 96 (Previously Presented) A semiconductor memory device according to claim 92, wherein a height of said cylinder type storage electrode is larger than its width.

Claim 97 (Previously Presented) A semiconductor memory device according to claim 92, wherein said cylinder type storage electrode has an inner wall and an outer wall facing said opposing electrode via a capacitor insulating film.

Claim 98 (Previously Presented) A semiconductor memory device according to claim 92, wherein said cylinder type storage electrode has an inner wall and an outer wall facing said opposing electrode via a capacitor insulating film.

Claim 99 (Previously Presented) A semiconductor memory device according to claim 92, further comprising wirings, formed over said second insulator, electrically connected to said second and fourth conductors respectively.

Claim 100 (Previously Presented) A semiconductor memory device according to claim 92, further comprising:

a fourth contact hole, formed through said second and first insulators, exposing a surface of said semiconductor substrate, and

a fifth conductor filled in said fourth contact hole,

wherein said third conductor is disposed in said first insulator, and a depth of said fourth contact hole is larger than said depth of said third contact hole.

Claim 101 (Previously Presented) A semiconductor memory device according to claim 92, wherein another of said impurity doped regions of said memory cell transistor is electrically connected to a bit line which is composed of lower conductive layer than said cylinder type storage electrode.

Claim 102 (Previously Presented) A semiconductor memory device according to claim 92, wherein said opposing electrode is composed of a different conductive material from a conductive material of said third conductor.

Claim 103 (Previously Presented) A semiconductor memory device according to claim 92, wherein said opposing electrode is composed of a polysilicon, and said third conductor is a metal silicide.

Claim 104 (Previously Presented) A semiconductor memory device according to claim 92, further comprising a third insulator, disposed between said opposing electrode and said semiconductor substrate, having etching characteristics different from that of said second insulator.

Claim 105 (Previously Presented) A semiconductor memory device according to claim 92, wherein said third insulator is composed of a nitride film.

Claim 106 (Previously Presented) A semiconductor memory device according to claim 92, wherein said third conductor is covered with a nitride film.

Claim 107 (Previously Presented) A semiconductor memory device according to claim 92, wherein said first and second contact holes are located in a memory cell area, and said third contact hole is located in a peripheral circuit area.

Claim 108 (Previously Presented) A semiconductor memory device according to claim 92, wherein said memory cell transistor is formed in an active region defined by a field insulating film, and said active region intersects a bit line.